LETTER

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Design and fabrication of memory devices based on nanoscale polyoxometalate clusters

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Flash memory devices—that is, non-volatile computer storage media that can be electrically erased and reprogrammed—are vital for portable electronics, but the scaling down of metal–oxide–semiconductor (MOS) flash memory to sizes of below ten nanometres per data cell presents challenges. Molecules have been proposed to replace MOS flash memory[1], but they suffer from low electrical conductivity, high resistance, low device yield, and finite thermal stability, limiting their integration into current MOS technologies. Although great advances have been made in the pursuit of molecule-based flash memory[2], there are a number of significant barriers to the realization of devices using conventional MOS technologies[3–7]. Here we show that core–shell polyoxometalate (POM) molecules[8] can act as candidate storage nodes for MOS flash memory. Realistic, industry-standard device simulations validate our approach at the nanometre scale, where the device performance is determined mainly by the number of molecules in the storage media and not by their position. To exploit the nature of the core–shell POM clusters, we show, at both the molecular and device level, that embedding $[(Se(IV)O_3)_2]^{4-}$ as an oxidizable dopant in the cluster core allows the oxidation of the molecule to a $[Se(V)_2O_6]^{2-}$ moiety containing a {Se(V)–Se(V)} bond (where curly brackets indicate a moiety, not a molecule) and reveals a new 5+ oxidation state for selenium. This new oxidation state can be observed at the device level, resulting in a new type of memory, which we call 'write-once-erase'. Taken together, these results show that POMs have the potential to be used as a realistic nanoscale flash memory. Also, the configuration of the doped POM core may lead to new types of electrical behaviour[9–11]. This work suggests a route to the practical integration of configurable molecules in MOS technologies as the lithographic scales approach the molecular limit[12].

To engineer the flash memory devices, we selected a core–shell POM 'Dawson-like' archetype as the functional part of the switching node with the general formula $[M_{18}O_{54}(XO_n)_2]^{m-}$ (where M = Mo or W, X = P, S or Se, $n = 3$ or 4 and $m = 2 \rightarrow 8$). This is because the cluster has a nanoscale size (about $1.2 \times 1 \times 1$ nm), a wide accessible charge range to act as ideal trapped charges for flash memory, a configurable cluster core (that is, P, S, Se as possible dopants) and a high thermal stability (about 600 °C) to cope with the high temperatures associated with flash memory post-processing. With the thermal stability in mind we therefore used a tungsten-based rather than molybdenum-based core–shell cluster. Furthermore, the effect of various dopants was investigated by density functional theory (DFT) calculations, which helped us to understand the likely reactivity and electronic structure of the clusters[13], and hence to choose an appropriate heteroatom. After careful consideration of the synthetically realistic options we hypothesized that $\{Se(IV)O_3\}$ would provide the right balance of structural stability and electronic activity, leading us to conclude that the cluster anion $[W_{18}O_{54}(SeO_3)_2]^{4-}$ would be an ideal candidate to investigate the development of practical flash memory devices.

To explore this idea we set about synthesizing the core–shell cluster anion $[W_{18}O_{54}(SeO_3)_2]^{4-}$ (**1a**) via a dehydration reaction of the selenite containing cluster $[W_{18}O_{56}(SeO_3)_2(H_2O)_2]^{8-}$ (**precursor**) (see Supplementary Information). Notably, this cluster demonstrates exceptionally rich redox behaviour associated not only with the reduction of the metal oxide cluster $\{W_{18}O_{54}\}$ cage, but also with the oxidation of selenite templates at the cluster core; see Fig. 1.

To provide a first demonstration of a flash memory cell using POMs, a lateral geometry was used with a ~4-nm Si nanowire channel covered with a 4-nm SiO_2 insulator. This design, rather than a vertical flash memory cell, was chosen to provide easy access for the exploration of the intrinsic ability of the POM to form the switching component of a flash memory device (see Fig. 2). Nominally identical flash memory characteristics were demonstrated in an array of nine independent devices. We tested devices with different geometries and only those with a distance between the control gate and the nanowire channel of below 60 nm demonstrated reproducible flash memory behaviour. The fabrication process is described in full in the Supplementary Information.

Figure 2b demonstrates a shift in the threshold voltage (ΔV_T) of 1.1 ± 0.1 V from the bare nanowire to the same nanowire coated in POMs. A large negative voltage of –20 V was then used to inject charge into the POMs before the control gate was again swept to demonstrate drain current characteristics with a ΔV_T shift of 1.2 ± 0.1 V at low voltages. After a further pulse of +20 V, the drain current characteristics returned to the characteristics close to the original uncharged state. The present device geometry is not optimized, accounting for the high voltages

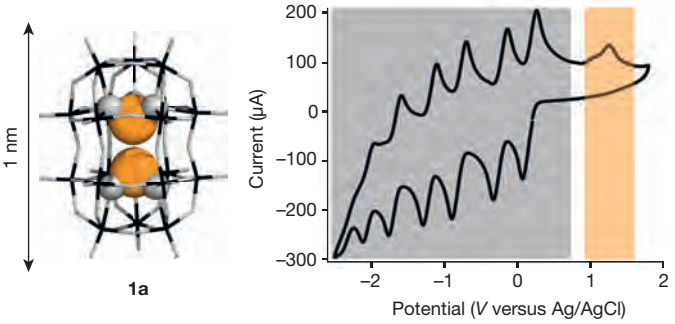

Figure 1 | Structure and electrochemical properties of compound 1a. On the left, the crystal structure of the core–shell cluster $[W_{18}O_{54}(SeO_3)_2]^{4-}$ (**1a**) is shown, with the $\{W_{18}O_{54}\}$ cage shown as black and grey lines. The two Se core dopants are shown as orange spheres. The cluster cage can be reduced multiple times (grey area) and the two Se dopants at the POM cluster core can be oxidized (orange area). On the right, the cyclic voltammetry is obtained from microcrystals of **1a** adhered to a glassy carbon electrode (diameter 1.5 mm) in 0.1 M tetrabutylammonium PF_6 acetonitrile solution at a scan rate of 200 mV s^{-1} and a scanning range V of −2.5 V to 1.8 V against a Ag/AgCl reference.

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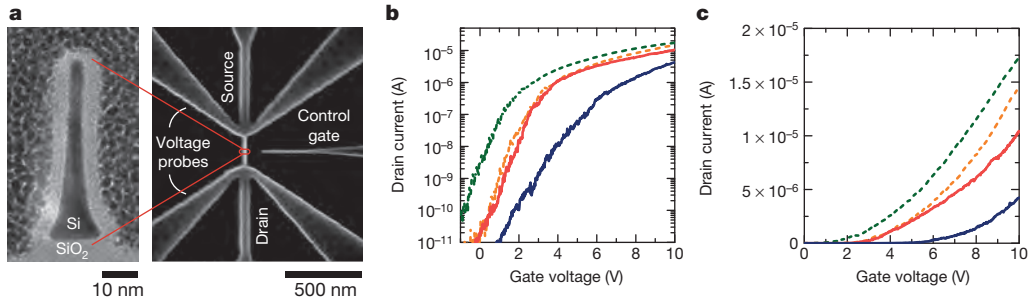


Figure 2 | Image of the flash memory device and the drain current behaviour with an applied voltage to the control gate. **a**, A cross-sectional transmission electron microscope (TEM) image (left) of the memory device with an SEM image (right) of the ~5-nm Si nanowire channel with side control gate. **b**, **c**, Measurements of the logarithmic (**b**) and linear (**c**) drain current versus gate voltage at 0.5 V source–drain voltage: before deposition of the POMs (green dashes), after the deposition of the POMs (orange dashes), after a −20 V pulse (blue line) and a +20 V pulse (red line). Panel **b** demonstrates depletion of the charge in the nanowire, resulting in a shift of the threshold voltage required to switch on the electrical conduction of the nanowire (orange dashed line) after **1a** was deposited around the nanowire. Therefore the control gate voltage required to produce the same drain current in the nanowire has moved to a higher voltage owing to the charge on the molecules of **1a**. The control gate was then used to charge and discharge the deposited molecules. −20 V was applied to the control gate, which charged the molecules around the nanowire, further increasing the control gate voltage required to produce the same drain current in the nanowire (solid blue lines in **b** and **c**). This effect could be reversed by applying a +20 V pulse to the control gate, which discharged the molecules and returned the control gate voltage for a fixed drain current to the original value with the uncharged **1a** molecules around the nanowire (red lines in **b** and **c**). The effect is repeatable, demonstrating a clear shift in the threshold voltage of the device when charged. The programming window (the threshold voltage change between the charged and uncharged **1a** molecules) is >1.2 V at low gate voltages.

required to write/erase but a plot of ΔV_T versus logarithmic time (see Supplementary Information) demonstrates that the present limit of the programme/erase times are 0.1 s and read times are 100 μs. The charge/discharge could be repeated many times and the retention time of the flash memory is at least 336 h, with the ultimate limit of the retention time expected to be significantly longer, given that no decay in the stored charge has yet been measured over the 336-h period. The read time is presently limited only by the *RC* time constant (the product of resistance

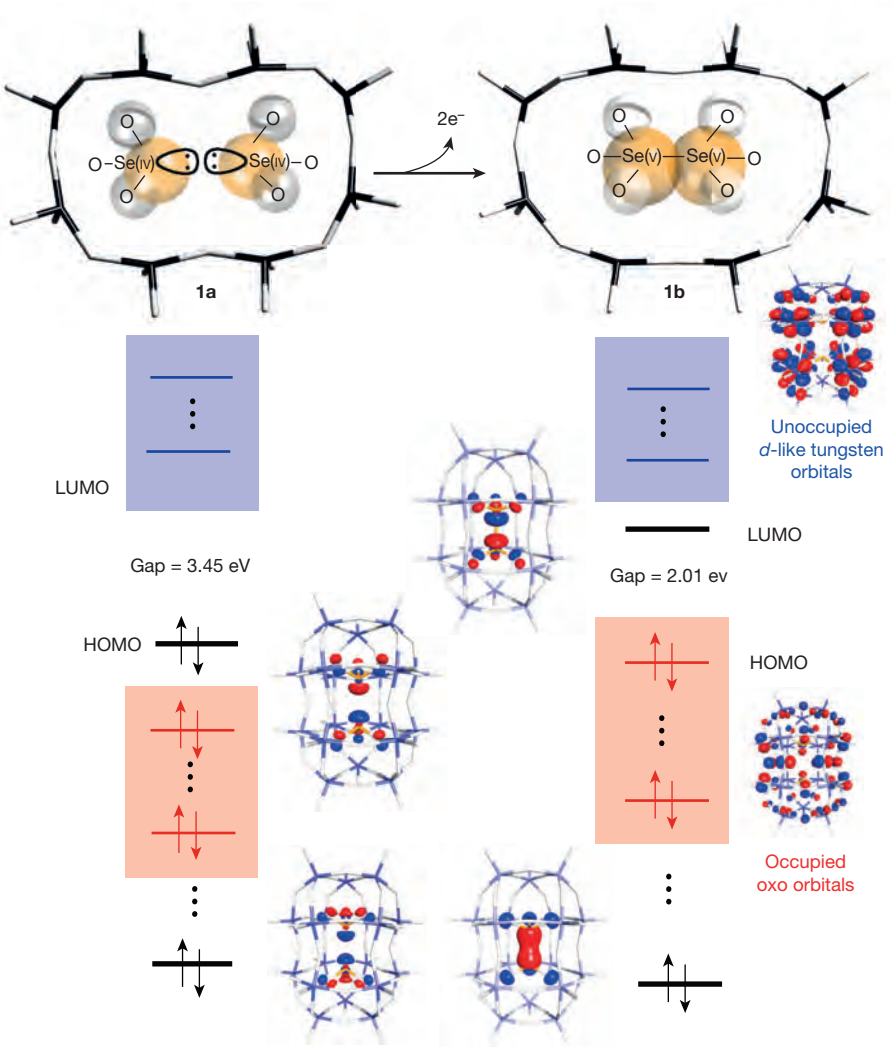
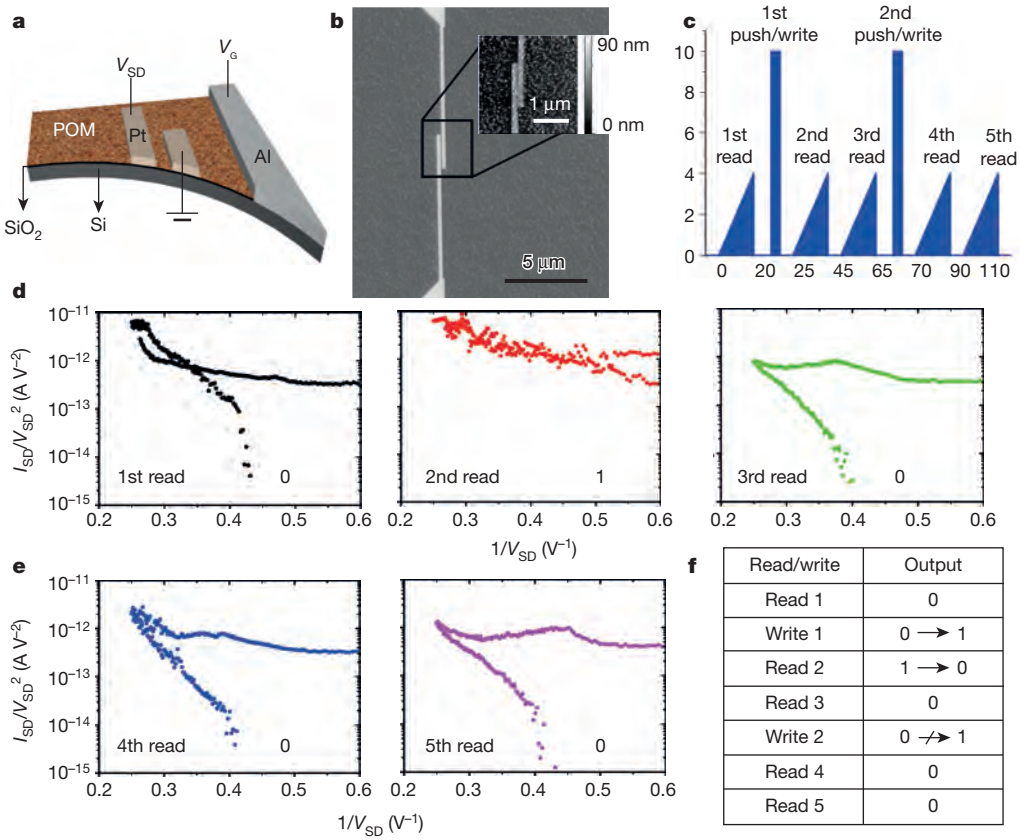


Figure 3 | Scheme depicting the formation of the Se(v)–Se(v) bond within the cluster cage. At the top, a schematic diagram shows the formation of the Se(v)–Se(v) bond in the transformation of **1a** to **1b**. At the bottom are the results from the DFT analysis, demonstrating the frontier orbitals and the formation of the Se(v)–Se(v) bond. Relevant orbitals delocalized over the Se moieties are highlighted in bold. The HOMO–LUMO gap is the energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). Although the orbital energies of POM clusters are separated by discrete energies, they can also be viewed as having a pseudoband-like orbital structure, and in this sense the blue box depicts the set of unoccupied tungsten *d*-like orbitals and the red box the set of occupied oxygen *p*-like orbitals.

and capacitance: 22.3 pF × 250 kΩ = 56 μs) of the nanowire devices and especially by the large pad capacitance. A radio-frequency design of the device and optimization of the capacitance and resistance should reduce this to subnanosecond read times. The write/erase time is limited by the large density of POM molecules (2×10^{15} cm^{-2}) and the current compliance of the characterization set-up. A device with a shorter distance from control gate to nanowire channel and significantly fewer POMs should reduce both the write/erase voltage and the time. Preliminary calculations suggest that 100 POMs would have a subpicosecond write time, subject to the device and characterization limits, but we expect the fundamental charging mechanisms of the POM to dominate at such device dimensions. The above analysis clearly demonstrates that the ultimate performance of the POM-based flash memory has not been reached and further work is required to determine the fundamental limits of the proposed technology. The sub-threshold slope for the −20 V pulsed measurements in Fig. 2b indicates additional charging mechanisms in the device in addition to the POM flash floating-gate mechanism. Because the POMs have been distributed over the entire device with high density, there are many potential charging mechanisms that could provide this type of non-optimal behaviour. The drain current characteristics after the +20 V pulse also indicate that the return to the original state of the POMs is not complete (Fig. 2b and c), suggesting that optimization of the device geometry and POM positioning is required to improve the performance. Nevertheless, these measurements demonstrate that it is possible to produce functional flash devices using POMs owing to their intrinsic *n*-type like properties simply by drop-casting a solution of the POM directly onto the gate architecture in a one-step process.

In addition to the exploitation of the shell of the POM clusters to trap charges for functional flash memory, we also investigated the role of the two inner 'core' moieties in the POM cluster archetype $[W_{18}O_{54}(XO_n)_2]^{m-}$ using DFT (where X is P, S or Se) to see whether it is possible to use these heteroatom dopants to change the electronic structure of the cluster using a redox process. This is because, in this cluster type, the heteroatoms are perfectly positioned next to each other to interact via their lone pairs of electrons. This is particularly true for compound **1a** because the two inner {Se(IV)O_3} moieties within the outer cluster shell have significant intramolecular non-bonded interactions, with a Se(IV)···Se(IV) distance of 3.1 Å; see Fig. 3.

This was confirmed by a DFT study, which showed that the ejection of two electrons from the cluster core should lead to an oxidation state change (Se(IV) → Se(V)) in **1a** commensurate with the formation of a Se–Se bond within the cluster. Not only is this redox process revealed by the electrochemical data (see Fig. 1 and Supplementary Information), the two-electron oxidation of **1a** to **1b** was confirmed directly by coulometry (see Supplementary Information), and the formation of a Se–Se bond is consistent with studies showing that the two-electron oxidized species is diamagnetic, as confirmed by electron paramagnetic resonance spectroscopy. In addition, the theoretical estimation of the reduction potentials are in good agreement with the experimental values, as are the theoretical values for the two-electron oxidation process leading to the formation of **1b** (see Supplementary Information).



Read/write	Output
Read 1	0
Write 1	0 → 1
Read 2	1 → 0
Read 3	0
Write 2	0 ↛ 1
Read 4	0
Read 5	0

Figure 4 | The write-once-erase device. Conceptual sketch (**a**) and SEM/AFM images (**b**) of the fabricated nano-gap electrodes coated with **1a**. **c**, The measurement procedure in terms of the applied voltage. The sample was subjected to a high-voltage push pulse applied between the source and drain electrodes on the surface of the sample, and then measured at a lower voltage level. The data are obtained by sweeping the source–drain voltage (V_{SD}) between the surface electrodes from 0 V to 4 V and back to 0 V with the substrate gate voltage maintained constant at 3 V. I_{SD} is the source–drain current and V_G is the gate voltage. **d**, **e**, Fowler–Nordheim[16,17] plots of the current–voltage data of the POM-covered nano-gap electrodes, which demonstrate whether trap states which can hold charge for a memory device are present between the two source and drain electrodes (when there is hysteresis between the forward and reverse voltage sweeps, trapped charge is present). For the '0' memory state, the hysteresis in the Fowler–Nordheim plots indicates trapped charge inside the gap between the electrodes. We observe that subjecting the system to excitation with source–drain voltage at 9–10 V changes the nature of the electron transport between the source and drain upon subsequent inspection, removing the hysteresis as shown for the memory state '1'. In this measurement, the effect is transient; disappearing after the first post-excitation probe, as shown conceptually in the table in panel **f**.

To explore whether we could use the oxidative behaviour expected for the Se-embedded cluster, we fabricated a nano-electronic device incorporating **1a** to test the predictions made by the theoretical analysis. An array of parallel Pt electrodes with a gap of approximately 50 nm was produced on a highly doped silicon substrate with a thermally grown 30-nm-thick barrier oxide. Sixty-four individual electrode pairs were fabricated on each sample. A contact was opened to the silicon substrate, allowing it to function as a gate electrode. Figure 4 demonstrates scanning electron microscopy (SEM) and atomic force microscopy (AFM) images of a fabricated electrode pair, after deposition of the POM material. Through high-volume control measurements (a total of more than 250 measurements were performed on electrode pairs with and without POMs) we verified that this system is capable of probing the electrical characteristics of cluster **1b**. To do this, control experiments were undertaken with no POM material present and samples using cluster **2**, $[W_{18}O_{56}(WO_6)]^{10-}$, which has a $\{W_{18}O_{54}\}$ shell identical to that of cluster **1**, but this time contains an oxidatively inactive $\{WO_6\}$ 'core' (see Supplementary Information). These studies demonstrated that subjecting **1a** to an excitation at high source–drain bias enabled us to influence the transport characteristics upon subsequent probing at lower voltages. Figure 4 shows measurements performed with a source–drain bias of up to 4 V both before and after subjecting the system to a source–drain bias of 9–10 V. Two measurements were performed after excitation and the procedure was repeated twice, with the gate bias kept at +3 V throughout the experiment. The measurements were deliberately carried out using a slow process ensuring maximum resolution of the analyser equipment, with a full probe measurement taking approximately 20 min. Retention and dissipation of the 'write' procedure are also on this timescale and the intrinsic rate limits are expected to be similar to those of the flash memory.

Significant hysteresis is observed between the upwards and downwards voltage sweeps, with a gap of approximately 0.2 V. This is also evident in the control measurements of cluster **2** and this device thus also proves that compounds **1** and **2** are perfect examples of trapped charges giving flash-memory-like behaviour consistent with our previous observations. For the first initial post-excitation measurement however, hysteresis is not observed for compound **1a**. Absence of the hysteresis indicates a modification of the transport across and between molecules to allow easier electron flow. We therefore consider the phenomenon to be a direct representation of the electrochemically observed oxidation process Se(IV) → Se(V). This effect was observed only after the initial excitation and cannot be recreated with consecutive pushing pulses. This was typical behaviour across several devices and implies that compound **1a** can be used as a 'write-once-erase' memory. As such the positive voltage driving force for this behaviour can be directly linked to the non-reversible oxidation process of the two Se guest atoms within the POM, demonstrating how, at the device level, the molecular configuration and formation of the Se(V) dopant underpins this unprecedented behaviour.

To evaluate the possibility of incorporation of $[W_{18}O_{54}(SeO_3)_2]^{4-}$ (**1a**) and $[W_{18}O_{56}(WO_6)]^{10-}$ (**2**) molecules to achieve realization of a floating gate (see Fig. 5) in a non-volatile molecular memory, we developed a multi-scaled, multi-level computational framework designed to perform realistic flash memory cell modelling to substantially extend our previous concept[14]. Here we simulate a flash cell design with shallow trench insulation[15], which is based on a transistor with a gate length of 18 nm and gives much more accurate results, allowing us to evaluate our devices for practical implementation. Our simulation workflow links the DFT results, which are presented above, to mesoscopic (continuous) transistor simulations with the commercial three-dimensional numerical device simulator GARAND (Gold Standard Simulations Limited). The motivation for using this hierarchy of modelling approaches is the complexity of the problem. Accurate description of the POM clusters requires first-principles calculations on the atomic level, involving around 100 atoms, while the descriptions of the current flow through the flash memory cell demands continuous modelling, applied to a system of millions of atoms (see Supplementary Information).

The first step in our computational approach is to replace the poly-Si floating gate with a layer of POM molecules (Fig. 5a). More specifically, we incorporated spatial charge distributions of either a **1a** or **2** molecule for different redox states (obtained from DFT calculations) into the flash cell device structure. The POMs are negatively charged and in the native state, and those charges are counterbalanced by positively charged cations. Similar to the atomic charges, the presence of the cations

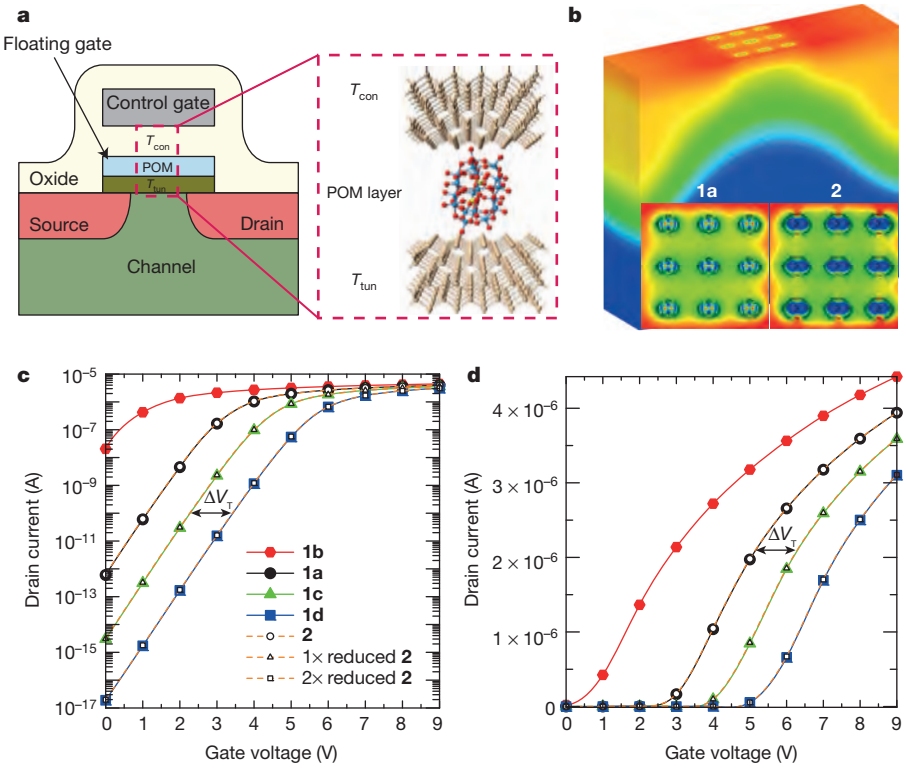


Figure 5 | Device modelling simulations of compounds 1a and 2. a, Schematic diagram representation of a single-transistor non-volatile memory cell, indicating the aimed substitution of the poly-Si floating gate with an array of POM clusters. T_{con} is the thickness of the control oxide and T_{tun} is the thickness of the tunnelling oxide. **b**, The three-dimensional electrostatic potential in the lower part of the oxide and the substrate, and two-dimensional map of the potential across the plane through the centre of the POMs, arranged in a 3 × 3 regular grid 4.5 nm from the Si–SiO_2 interface for the compounds **1a** and **2**, as schematically illustrated. **c**, **d**, Drain current versus gate voltage with a drain bias of 50 mV in logarithmic (**c**) scale and linear (**d**) scale for a bulk molecular flash cell: 2× oxidized $[W_{18}O_{54}(SeO_3)_2]^{2-}$ (**1b**), $[W_{18}O_{54}(SeO_3)_2]^{4-}$ (**1a**), 1× reduced $[W_{18}O_{54}(SeO_3)_2]^{5-}$ (**1c**) and 2× reduced $[W_{18}O_{54}(SeO_3)_2]^{6-}$ (**1d**), in comparison with $[W_{18}O_{56}(WO_6)]^{10-}$ (**2**), 1× reduced $[W_{18}O_{56}(WO_6)]^{11-}$ and 2× reduced $[W_{18}O_{56}(WO_6)]^{12-}$. V_T is the threshold voltage.

in the POM layer is modelled as a set of fractional point charges distributed around each POM. The total positive charge balances out the negative charge of the parent POMs, so that any reduction/oxidation of the POM would lead to the presence of extra electron charges in the gate stack. This provides localized balancing of each POM, essential for modelling a flash cell with broad dispersion of the position and number of POMs in the gate dielectric (see Supplementary Information).

Assuming that the POM layer consists of nine **1a** molecules arranged in a three-by-three array, we were able to evaluate the non-volatile molecular memory performance with the help of the GARAND simulator. Figure 5b shows the three-dimensional electrostatic potential in the lower part of the oxide and the substrate. In addition, the two-dimensional map of the potential across the plane through the centre of the POM layer (as arranged in a 3×3 regular grid) is presented in the same figure. From our calculations, we were able to obtain not only qualitative but also quantitative information on the impact of the oxidation/reduction of the **1a**/**2** molecular layer on the flash cell characteristics. In the process of evaluating the performance of each flash cell, the drain current I_D versus gate voltage V_G characteristic presented in Fig. 5c has an important role. Figure 5c, d shows the impact of the oxidation/reduction of the **1a**/**2** floating-gate layer on the drain current and threshold voltage of the flash memory cell. Clearly, adding electrons to the POMs leads to reduction of the OFF-current (the current value at $V_G = 0.0$ V). This is based on the fact that introducing more negative charge in the floating gate repels the electrons from the channel of the transistor. As a result, the OFF-current is reduced because it is directly influenced by the electron density distribution in the channel of the transistor (fewer electrons in the channel means less current). More importantly, the two types of POM give exactly identical I_D–V_G characteristics. The reason for this is that even though **1a** and **2** have different local charge distributions (clearly visible in the two-dimensional electrostatic potential plot in Fig. 5b), the size of each POM is very small in comparison to the channel area. Therefore, the source-to-drain current is almost unaffected by variation of the local charge distribution in the **1a** and **2** molecules. This effect is expected to increase with scaling down the channel area.

We can conclude from the results based on our multi-level computational framework that POM molecules can serve as a floating gate, with the potential for significant applications in molecular-based flash memory cells. The results demonstrate a significant programming window between each bit with a high signal-to-noise ratio. Another important characteristic for each device is the ratio of the OFF-current to the ON-current (the current at $V_G = 0.9$ V). This current ratio increases with increasing oxidation state of the POM molecule (Fig. 5c). For the clusters $[W_{18}O_{54}(SeO_3)_2]^{2-}$ (**1b**)/$[W_{18}O_{56}(WO_6)]^{10-}$ (**2**), we calculate an increase in the ratio of around two to six orders of magnitude, whereas for $[W_{18}O_{54}(SeO_3)_2]^{6-}$ (**1d**)/$[W_{18}O_{56}(WO_6)]^{12-}$, we observe a difference spanning eleven orders of magnitude.

Online Content Methods, along with any additional Extended Data display items and Source Data, are available in the online version of the paper; references unique to these sections appear only in the online paper.

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1. Joachim, C., Gimzewski, J. K. & Aviram, A. Electronics using hybrid-molecular and mono-molecular devices. *Nature* **408,** 541–548 (2000).
2. Shaw, J. T. *et al.* Integration of self-assembled redox molecules in flash memories. *IEEE Trans. Electron. Dev.* **58,** 826–834 (2011).
3. Zhu, H. *et al.* Non-volatile memory with self-assembled ferrocene charge trapping layer. *Appl. Phys. Lett.* **103,** 53102–53104 (2013).
4. Chen, P.-C., Shen, G. & Zhou, C. Chemical sensors and electronic noses based on 1-D metal oxide nanostructures. *IEEE Trans. Nanotechnol.* **7,** 668–682 (2008).
5. Shaw, J., Xu, Q., Rajwade, S., Hou, T.-H. & Kan, E. C. Redox molecules for a resonant tunneling barrier in nonvolatile memory. *IEEE Trans. Electron. Dev.* **59,** 1189–1198 (2012).
6. Seol, M.-L., Choi, S.-J., Kim, C.-H., Moon, D.-I. & Choi, Y.-K. Porphyrin-silicon hybrid field-effect transistor with individually addressable top-gate structure. *ACS Nano* **6,** 183–189 (2012).
7. Tans, S. J., Verschueren, A. R. M. & Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **393,** 49–52 (1998).
8. Long, D. L. & Cronin, L. Towards polyoxometalate integrated nanosystems. *Chem. Eur. J.* **12,** 3698–3706 (2006).
9. Lehmann, J., Gaita-Arino, A., Coronado, E. & Loss, D. Spin qubits with electrically gated polyoxometalate molecules. *Nature Nanotechnol.* **2,** 312–317 (2007).
10. Li, H. *et al.* Layer-by-layer assembly and UV photoreduction of graphene–polyoxometalate composite films for electronics. *J. Am. Chem. Soc.* **133,** 9423–9429 (2011).
11. Fleming, L. *et al.* Surface-mediated reversible electron transfer reactions within a molecular metal oxide nano-cage. *Nature Nanotechnol.* **3,** 229–233 (2008).
12. Bonfiglio, V. & Iannaccone, G. Sensitivity-based investigation of threshold voltage variability in 32-nm flash memory cells and MOSFETs. *Solid-State Electron.* **84,** 127–131 (2013).
13. Vilà-Nadal, L. *et al.* Polyoxometalate $\{W_{18}O_{56}XO_6\}$ clusters with embedded redox-active main-group templates as localized inner-cluster radicals. *Angew. Chem. Int. Ed.* **52,** 9695–9699 (2013).
14. Vilà-Nadal, L. *et al.* Towards polyoxometalate-cluster-based nano-electronics. *Chem. Eur. J.* **19,** 16502–16511 (2013).
15. Gallon, C. *et al.* Electrical analysis of mechanical stress induced by STI in short MOSFETs using externally applied stress. *IEEE Trans. Electron. Dev.* **51,** 1254–1261 (2004).
16. Simmons, J. G. Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film. *J. Appl. Phys.* **34,** 1793–1803 (1963).
17. Fowler, R. H. & Nordheim, L. Electron emission in intense electric fields. *Proc. R. Soc. Lond. A* **119,** 173–181 (1928).

Supplementary Information is available in the online version of the paper.

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Author Contributions L.C. conceived the idea, designed the project and coordinated the efforts of the research team. J.Y. synthesised the clusters and conducted the first electrochemistry experiments and structural characterization with D.-L.L. H.N.M., C.B., L.V.-N., and L.C. helped to characterize the physical properties of the clusters. C.B. did the electron paramagnetic resonance, electrochemistry and spectroscopic measurements. L.V.-N., L.C., V.P.G. and A.A. designed the theory-to-modelling strategy. L.V.-N., with J.M.P., did the DFT calculations. V.P.G. and A.A. did the device simulation. R.H.P. and N.G. fabricated and characterized the electrode arrays, produced the devices, made the measurements and characterized the data. M.M.M. and D.J.P. designed the nanowire arrays and M.M.M. fabricated the electrodes and optimized the data with D.J.P., who helped analyse the results. C.B., L.V.-N. and L.C. co-wrote the paper with input from all the authors.

Author Information Atomic coordinates for the reported crystal structures have been deposited with the Cambridge Structural Database under the accession codes 997534 (compound **precursor**), 997535 (compound **1a**), 997536 (compound **1c**) and 997537 (compound **1d**), and full synthetic, electrochemical, device theory, device modelling and electronic device data is given in the Supplementary Information. Reprints and permissions information is available at www.nature.com/reprints. The authors declare no competing financial interests. Readers are welcome to comment on the online version of the paper. Correspondence and requests for materials should be addressed to L.C. (lee.cronin@glasgow.ac.uk).